# 2-wire Remote I/O Expander CH423

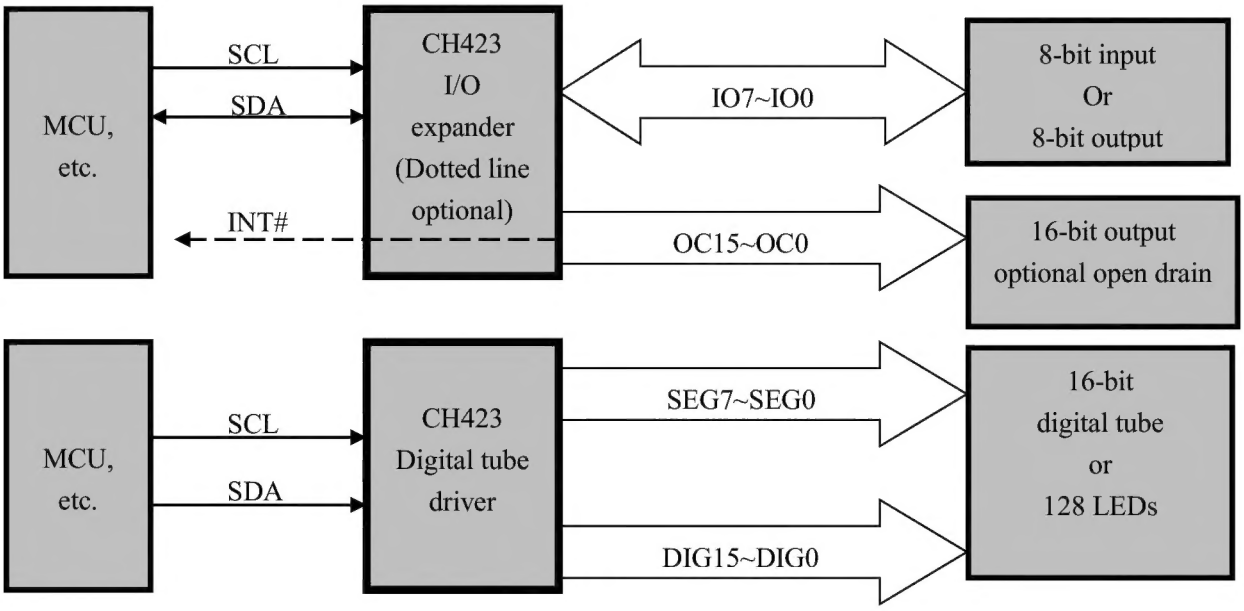
Datasheet

Version: 2B

https://wch-ic.com

## 1. Overview

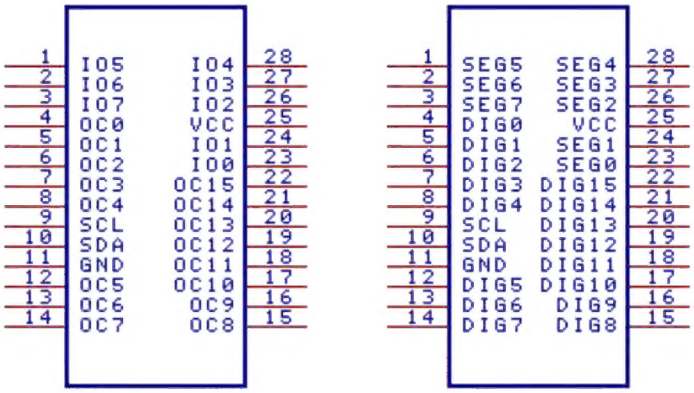
CH423 is a general remote I/O expander with 2-wire serial interface. CH423 provides 8 bidirectional input and output pins and 16 general-purpose output pins, supporting input level change interrupts; CH423 has a built-in current drive circuit that can statically drive 24 LEDs or dynamically drive 128 LEDs (equivalent to 16 digital tube). CH423 exchanges data with MCU through a 2-wire serial interface.




## 2. Features

- 8 general-purpose I/O pins, GPIOs and 16 general-purpose output pins, GPOs, can be remotely expanded through a 2-wire serial interface.
- Built-in current driver stage, continuous drive current is not less than 15mA, and OC pin outputs 1/16 pulse sink current is not less than 120mA.
- The static display driving mode supports 24 LEDs or 3-bit common anode digital tubes.
- The time-sharing dynamic scanning display driver mode supports 128 LEDs or 16-bit common cathode digital tubes, and supports brightness control.
- The bidirectional I/O pin has the function of generating an interrupt when the input level changes in input mode, and the interrupt output is active low.
- The 16 general-purpose output pins can be selected as push-pull output or open-drain output.
- Support 3V ~ 5V power supply voltage, support low-power sleep, and can be awakened by input level changes.
- High-speed 2-wire serial interface, clock speed from 0 to 1MHz, compatible with 2-wire I2C bus, saving pins.
- Available in DIP28S and SOP28 lead-free packages, RoHS compliant.

## 3. Packages




| Package form | Shaping width | | Pin spacing | | Package description | Order model |
|---|---|---|---|---|---|---|
| SOP28 | 7.62mm | 300mil | 1.27mm | 50mil | Small Outline Package | CH423S |
| DIP28S<br>SK-DIP28 | 7.62mm | 300mil | 2.54mm | 100mil | Skinny dual in-line package | CH423A |

*Note: CH423D in SDIP28 package (pin pitch 1.78mm) has been discontinued. Please give priority to using chip packaging form.*

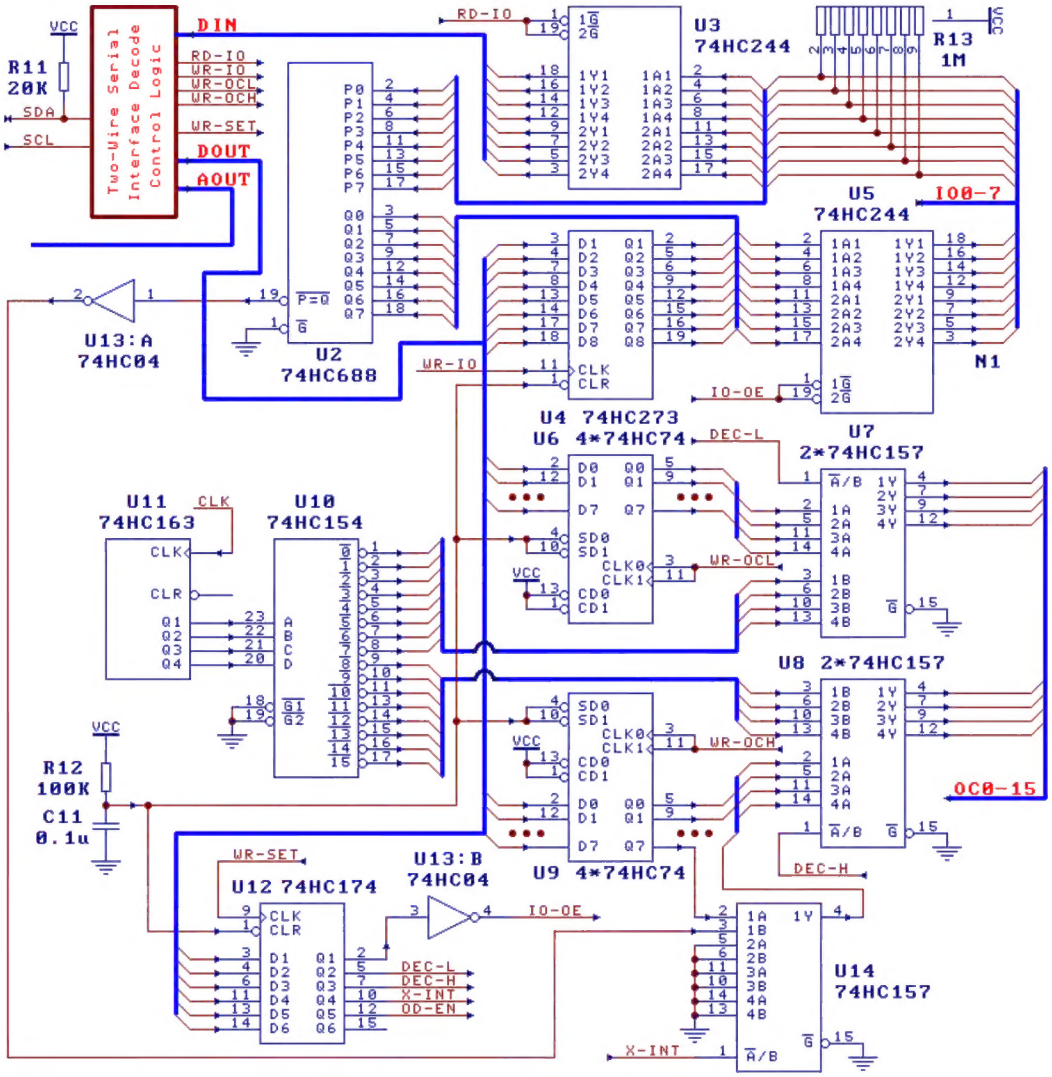
## 4. Pin Definitions

| Pin No. | Pin name | Type | Pin description |
|---|---|---|---|
| 25 | VCC | Power supply | Positive power supply, continuous current is not less than 150mA |
| 11 | GND | Power supply | Common ground, continuous current not less than 150mA |
| 23,24,26,<br>27,28,1,2,3 | IO0~IO7 | Three-state output and input | Bidirectional input and output, built-in weak pull-up resistor<br>During dynamic scanning, it is the segment driver of the common cathode digital tube, and active high. |
| 4~8/<br>12~22 | OC0~OC15 | Push-pull or open-drain output | General output, optional open-drain output, active low level<br>During dynamic scanning, it is the word driver of the common cathode digital tube, active low. |
| 10 | SDA | Open-drain output and input | Data input and output for 2-wire serial interface with built-in pull-up resistors |
| 9 | SCL | Input | Data clock for 2-wire serial interface |

# 5. Functional Specification

## 5.1 Internal Circuit Principle

(For explaining functions, excluding dynamic drivers, for reference only)




## 5.2 General Instructions

The data in this manual are binary numbers ending with B, hexadecimal numbers ending with H, otherwise they are decimal numbers. The bit marked x indicates that the bit can be any value.

MCU (can also be a CPU, DSP, microprocessor, MCU and other controllers) controls the CH423 chip through a 2-wire serial interface. The 2-wire serial interface of CH423 is implemented by hardware. The MCU can frequently control the CH423 chip through the serial interface. High-speed operation without reducing the working efficiency of CH423.

## 5.3 Bidirectional I/O Pins

The IO7 ~ IO0 pins of CH423 are bidirectional input and output pins. The default is the input direction, which is used to input the current status of the external pin. When set to the output direction, it can output high and low levels to drive the LED light-emitting tube or perform I/O extension.

In the dynamic scan display driving mode, the IO7 ~ IO0 pins can be used to drive each segment pin of the digital tube. Since CH423 can limit the segment drive current internally, the external series segment current limiting resistor

can be omitted.

## 5.4 General-purpose Output Pins

The OC15~OC0 pins of CH423 are push-pull or open-drain output pins, and the default is push-pull output.
After selecting the open-drain output mode, there are only two states of outputting low level and no output. It cannot output high level. The default is no output state.
In the dynamic scan display driving mode, the OC15 ~ OC0 pins can be used to drive each common terminal of the common cathode digital tube, and can absorb a large sink current in a pulse manner.
If you only drive 8-bit digital tubes, the remaining 8 general-purpose output pins can still be used for GPO.

## 5.5 Level Change Interrupt

If the input level change interrupt is allowed, then the OC15 pin of CH423 will be used as an interrupt request output pin, and the low level is active.
When the IO7~IO0 pins of CH423 are used for input, they can support input level change interrupts. The input level change refers to the detection of the current status input from the IO7~IO0 pins and the pre-written output register of the IO7~IO0 pins. The data in (U4 in the figure) is different. If the above changes are detected (U2 in the figure is the comparator), then CH423 will output an active low-level interrupt through the OC15 pin until the MCU rewrites the output register of the IO7~IO0 pins, and the new value is the same as the slave IO7 ~ When the current status of the IO0 pin input is the same, the OC15 pin of CH423 returns to high level or does not output.

## 5.6 Power-on Reset

CH423 has a built-in power-on reset circuit (R12 and C11 in the figure), which is used to restore each internal register to the default state when the chip is just powered on. For example, after each power-on, the bidirectional input and output pins are in the input state, and the general-purpose output pins are in the high-level state.

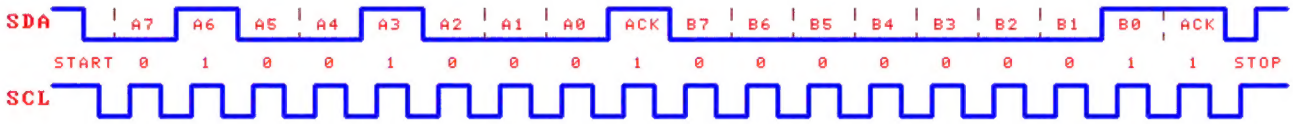
## 5.7 Serial Interface

CH423 has a hardware-implemented 2-wire serial interface, including 2 signal lines: serial data clock input line SCL, serial data input and output line SDA.
SDA is a quasi-bidirectional signal line with a pull-up resistor, and the default is high level. SDA is used for serial data input and output. A high level indicates bit data 1, and a low level indicates bit data 0. The order of serial data input is high bit first, low bit last.
SCL is the input signal line, which defaults to high level. SCL is used to provide the serial clock. CH423 inputs data from SDA on its rising edge and outputs data from SDA on its falling edge.
The falling edge of SDA that occurs while SCL is high is defined as the start signal of the serial interface, and the rising edge of SDA that occurs while SCL is high is defined as the stop signal of the serial interface. CH423 only receives and analyzes commands after detecting the start signal. Therefore, when the I/O pin resources of the MCU are tight, the SCL pin can be shared with other interface circuits while keeping the SDA pin state unchanged; Both the SCL pin and the SDA pin can be shared with other interface circuits if it can be ensured that changes to the SDA pin only occur during periods when the SCL pin is low.
The communication process between the MCU and CH423 is always divided into 6 steps, which are divided into two types according to the operation direction of the MCU, one is a write operation, used to output data, and the other is a read operation, used to input data. For the specific process, please refer to the instructions in the routines.
The write operation includes the following 6 steps: output start signal, output byte 1, response 1, output byte 2, response 2, and output stop signal. Among them, the start signal and stop signal are as mentioned above, response 1 and response 2 are always fixed to 1, and output byte 1 and output byte 2 each contain 8 data bits, that is, one byte

of data.

The read operation includes the following 6 steps: output start signal, output byte 1, response 1, input byte 2, response 2, and output stop signal. Among them, the start signal and stop signal are as mentioned above, response 1 and response 2 are always fixed to 1, and output byte 1 and input byte 2 each contain 8 data bits, that is, one byte of data.

The following figure shows an example of a write operation, where byte 1 is 01001000B, or 48H, and byte 2 is 00000001B, or 01H.




## 5.8 Dynamic Drive Digital Tube

CH423 can dynamically drive 16 common cathode digital tubes. After the same segment pins (segment A~segment G and decimal point) of all digital tubes are connected in parallel, they are connected to the segment drive pins of CH423 through 8 series-connected current-limiting resistors R1~R8. IO7~IO0, the common cathodes of each digital tube are driven by the OC15~OC0 pins of CH423 respectively. The resistor RN8 connected in series with the segment pin is used to limit and balance the segment drive current. Under a 5V power supply voltage, a 270Ω resistor connected in series usually corresponds to a segment current of 10mA. CH423 can be connected to an 8×16 matrix LED array or 128 independent light-emitting tubes, or it can support common anode digital tubes through an external inverting driver, or it can support large-size digital tubes through an external high-power tube. Please refer to the CH452 data sheet. method in.

CH423 has 16 8-bit data registers inside (equivalent to 16 U4 in the figure), which are used to save 16 words of data, corresponding to the 16 digital tubes driven by CH423 or 16 groups of 8 light-emitting diodes each. Bits 7 to 0 of the word data in the data register correspond to the decimal points and segments G to A of the eight digital tubes respectively. For the LED array, the data bits of each word data uniquely correspond to one LED. When the data bit is 1, the corresponding segment or luminous tube of the digital tube will light up; when the data bit is 0, the corresponding segment or luminous tube of the digital tube will go out. For example, bit 0 of the third data register is 1, so segment A of the corresponding third digital tube lights up. The picture below shows the segment names of the digital tube.

# 6. Operation Command

The operation commands of CH423 are divided into 6 groups. The start signal, stop signal, response 1 and response 2 of each command are the same. The difference lies in the different data of output byte 1 and byte 2 and the different transmission direction of byte 2. Byte 1 is used for 2-wire serial port control logic, or for generating addresses (AOUT bus in the figure), and byte 2 is used for input and output data (DIN and DOUT buses in the figure).

## 6.1. Set System Parameter Command (WR-SET control line in the picture)

The output byte 1 of this command is 01001000B, i.e. 48H; this command can support 7 system parameters, and the output byte 2 is [SLEEP][INTENS][OD_EN][X_INT][DEC_H][DEC_L][IO_OE]B.

Set system parameter command is used to set the system-level parameters of CH423 (written to U12 in the figure): output enable IO_OE for bidirectional input and output pins IO7~IO0, dynamic scan enable DEC_L for output pins OC7~OC0, output The dynamic scan enable DEC_H of pins OC15~OC8, the input level change interrupt enable X_INT, the open-drain output enable OD_EN of the output pins OC15~OC0, the dynamic display driver brightness control INTENS, and the low-power sleep control SLEEP. After power-on reset, the above parameters default to 0.

IO_OE is used to control the three-state output of the bidirectional input and output pins IO7~IO0. When it is 0, the output is disabled (used for input through U3 in the figure), and when it is 1, the output is allowed (U5 output in the figure).

DEC_L is used to control the dynamic scan enable of the output pins OC7~OC0. When it is 0, OC7~OC0 is used for the general output of I/O expansion (select U6 in the figure). When it is 1, OC7~OC0 are translated by the timing scan counter. Post-code control (select U10 in the figure), select one of the OC7 ~ OC0 pins to output low level at the same time, and the other pins do not output, which is used to realize time-sharing display driving.

DEC_H is used to control the dynamic scan enable of the output pins OC15~OC8. When it is 0, OC15~OC8 is used for the general output of I/O expansion (select U9 in the figure). When it is 1, OC15~OC8 are translated by the timing scan counter. Post-code control (select U10 in the figure), select one of the OC15 ~ OC8 pins to output low level at the same time, and the other pins do not output, which is used to realize time-sharing display driving.

X_INT is used to enable the input level change interrupt (U14 in the control figure). When it is 0, it disables the level change interrupt. When it is 1 and DEC_H is 0, it allows the output level change interrupt from the OC15 pin (U2 in the diagram generated by comparison).

OD_EN is used to enable the open-drain output of the output pins OC15~OC0. When it is 0, OC15~OC0 are push-pull outputs (can output low level and high level). When it is 1, OC15~OC0 are open-drain outputs (only Output low level and no output).

INTENS is used to control the brightness of the dynamic display driver. It contains two bits of data and has 4 combinations: data 00B, 01B, and 10B respectively set the display driver duty cycle to 4/4, 1/4, and 2/4, and enable the internal Segment driver current limit; Data 11B sets the display driver duty cycle to 4/4, but the internal segment driver current limit is prohibited, so the external current limit resistors R1~R8 need to be connected in series to the segment pins.

SLEEP is used to put CH423 into a low-power sleep state, thereby saving power. CH423 in low-power sleep state can be awakened by any of the following two events. The first event is the input level change, that is, the current status of the IO7 ~ IO0 pin input is different from the data previously written in the output register (U4 in the figure) of the IO7 ~ IO0 pin; the second event is receiving the next operation command issued by the MCU. When CH423 wakes up, the SLEEP bit will be automatically cleared to 0. The sleep and wake-up operations themselves will not affect other working states of CH423. If it is awakened by the previous event, a level change interrupt will be generated at the same time.

For example, when the output byte 2 is 17H, then OC15~OC0 dynamically drives 16 digital tubes in an open-drain

mode; when the output byte 2 is 03H, only OC7~OC0 dynamically drives 8 digital tubes, and the remaining OC15~OC8 still Used for general output GPO; when output byte 2 is 05H, only OC15 ~ OC8 dynamically drive 8 digital tubes, and the remaining OC7 ~ OC0 are still used for general output GPO.
This command does not affect the data in the output registers and internal data buffers of each pin.

### 6.2. Set Low 8-bit General Output Command (WR-OCL control line in figure)

The output byte 1 of this command is 44H, and the output byte 2 is [OC_L_DAT]B, that is, 8-bit data between 00H and 0FFH, which is used to write to the output register of the output pins OC7~OC0 (U6 in the figure) , writing 0 will make the pin output low level, writing 1 will make the pin output high level.

### 6.3. Set High 8-bit General Output Command (WR-OCH control line in figure)

The output byte 1 of this command is 46H, and the output byte 2 is [OC_H_DAT]B, that is, 8-bit data between 00H and 0FFH, which is used to write to the output register of the output pins OC15~OC8 (U9 in the figure) , writing 0 will make the pin output low level, writing 1 will make the pin output high level.

### 6.4. Set Bidirectional I/O Commands (WR-IO control line in figure)

The output byte 1 of this command is 60H, 62H, 64H, 66H, 68H, 6AH, 6CH, 6EH, 70H, 72H, 74H, 76H, 78H, 7AH, 7CH, 7EH, in which bits 4 to 1 are addresses and can be ignored; the output byte 2 is [IO_DAT]B, i.e., 8-bit data from 00H to 0FFH, which is used to write the output registers (U4 in the diagram) of bi-directional input/output pins IO7 to IO0. Output byte 2 is [IO_DAT]B, i.e., 8-bit data between 00H and 0FFH, which is used to write into the output registers of bi-directional input/output pins IO7 to IO0 (U4 in the figure). If the IO_OE is 1 to allow the output, then write 0 to make the pin output a low level, and write 1 to make the pin output a high level.

### 6.5. Load Word Data Command (used for automatic dynamic display driver of digital tube, the command code is the same as the command to set bidirectional I/O)

Byte 1 of this command is 011[DIG_ADDR]0B, i.e., 60H, 62H, 64H, 66H, 68H, 6AH, 6CH, 6EH, 70H, 72H, 74H, 76H, 78H, 7AH, 7CH, 7EH; byte 2 is [DIG_DATA]B, i.e., the value between 00H and 0FFH.
The load word data command is used to write the word data DIG_DATA into the data register at the address specified by DIG_ADDR. DIG_ADDR specifies the address of the data register through 4-bit data. Data 0000B~1111B specifies addresses 0~15 respectively, corresponding to the 16 digital tubes driven by the OC0~OC15 pins. DIG_DATA is 8-bit word data. For example, command data 01100000B, 01111001B means writing word data 79H into the first data register, so that the digital tube driven by the OC0 pin will display E.
The data in the CH423 internal data register is uncertain after power-on reset, so before turning on the display, you should clear the data in the data register or directly load the data to be displayed. The reset process does not affect the data in the data register.

### 6.6. Read Bidirectional I/O Commands (RD-IO control line in the picture)

The output byte 1 of this command is 01001101B, which is 4DH; the input byte 2 is the current pin status of the bidirectional input and output pins IO7~IO0.
The read bidirectional input and output command is used to obtain the current status of the IO7~IO0 pins. When IO_OE is 0, it is to obtain the input status, otherwise it is to obtain the output status. This command is a read operation and is the only command with data return. MCU must first release the SDA pin (three-state output is disabled or pulled up to high level), and then CH423 outputs the current pin status from the SDA pin.
When CH423 is used as a digital tube display driver, it can read the input status of 8 external buttons after temporarily turning off the display.

# 7. Parameters

## 7.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

| Name | Parameter description | Min. | Max. | Unit |
|---|---|---|---|---|
| TA | Ambient temperature during operation | -40 | 85 | ℃ |
| TS | Ambient temperature during storage | -55 | 125 | ℃ |
| VCC | Supply voltage (VDD connected to power supply, GND) | -0.5 | 6.0 | V |
| VIO | Voltage on the input or output pins | -0.5 | VCC+0.5 | V |
| IMoc | Continuous drive current for a single OC pin | 0 | 30 | mA |
| IMocp | 1/16 duty cycle pulse drive current for single OC pin | 0 | 150 | mA |
| IMio | Continuous drive current for a single IO pin | -25 | 25 | mA |
| IMall | The sum of the continuous drive currents of all IO pins or the sum of the continuous drive currents of all OC pins | 0 | 160 | mA |

## 7.2. Electrical Parameter

(Test conditions: TA=25℃, VCC=5V, if VCC=3.3V then multiply the current value in the table by 40%)

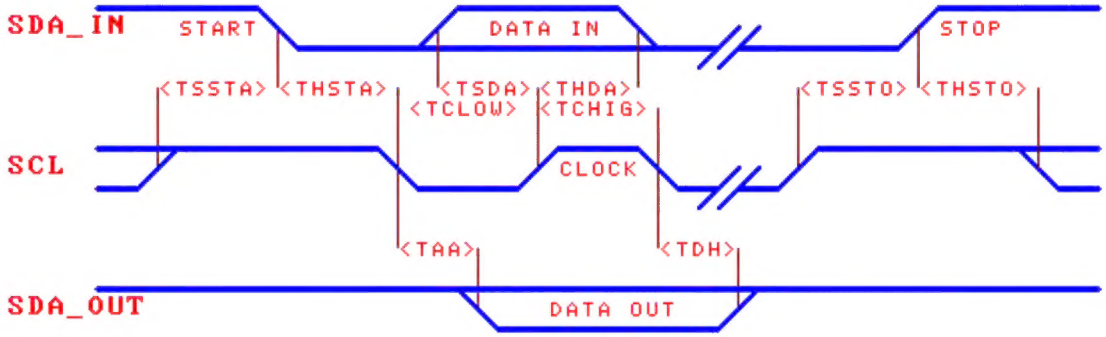
| Name | Parameter description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | System supply voltage | 2.9 | 5 | 5.3 | V |
| ICC | Working current | 0.1 | 80 | 120 | mA |
| ICCs5 | Quiescent current at 5V (SCL and SDA high) | | 0.4 | 0.9 | mA |
| ICCs3 | Quiescent current at 3.3V (SCL and SDA high) | | 0.1 | 0.3 | mA |
| VIL | SCL and SDA pin low level input voltage | -0.5 | | 0.8 | V |
| VIH | SCL and SDA high level input voltage | 2.0 | | VCC+0.5 | V |
| VILio | IO pin low level input voltage | -0.5 | | 0.6 | V |
| VIHio | IO pin high level input voltage | 1.9 | | VCC+0.5 | V |
| VOLoc | OC pin low level output voltage (-100mA) | | 0.6 | 0.8 | V |
| VOLoc | OC pin low level output voltage (-30mA) | | 0.2 | 0.3 | V |
| VOHoc | IO pin low level output voltage (-15mA) | VCC-0.5 | | | V |
| VOLio | IO pin high level output voltage (-15mA) | | | 0.5 | V |
| VOHio | IO pin high level output voltage (12mA，INTENS=11) | VCC-0.5 | | | V |
| VOHioL | IO pin high level output voltage (8mA，INTENS=00) | VCC-0.5 | | | V |
| VOL | SDA pin low level output voltage (-4mA) | | | 0.5 | V |
| IUP1 | Input weak pull-up current for IO pin | 1 | 5 | 10 | uA |
| IUP2 | Input pull-up current for SDA pin | 150 | 250 | 400 | uA |
| VR | Default voltage threshold for power-on reset | 2.3 | 2.6 | 2.9 | V |

## 7.3. Timing Parameter

(Test conditions: TA=25℃, VCC=5V, refer to the attached picture)

(Note: The measurement unit of this table is mainly nanoseconds, that is, 10-9 seconds. If the maximum value is not indicated, the theoretical value can be infinite)

| Name | Parameter description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| TPR | Reset time generated by power-on detection | 15 | 30 | 80 | mS |
| TSSTA | SDA falling edge start signal setup time | 100 | | | nS |
| THSTA | SDA falling edge start signal holding time | 100 | | | nS |
| TSSTO | SDA rising edge stop signal setup time | 100 | | | nS |
| THSTO | SDA rising edge stop signal holding time | 100 | | | nS |
| TCLOW | The low level width of the SCL clock signal | 100 | | | nS |
| TCHIG | The high level width of the SCL clock signal | 100 | | | nS |
| TSDA | SDA input data setup time for SCL rising edge | 30 | | | nS |
| THDA | SDA input data hold time for SCL rising edge | 10 | | | nS |
| TAA | SDA output data valid delay to SCL falling edge | 3 | | 30 | nS |
| TDH | SDA output data invalid delay to SCL falling edge | 3 | | 40 | nS |
| Rate | Average data transfer rate | 0 | | 1M | bps |

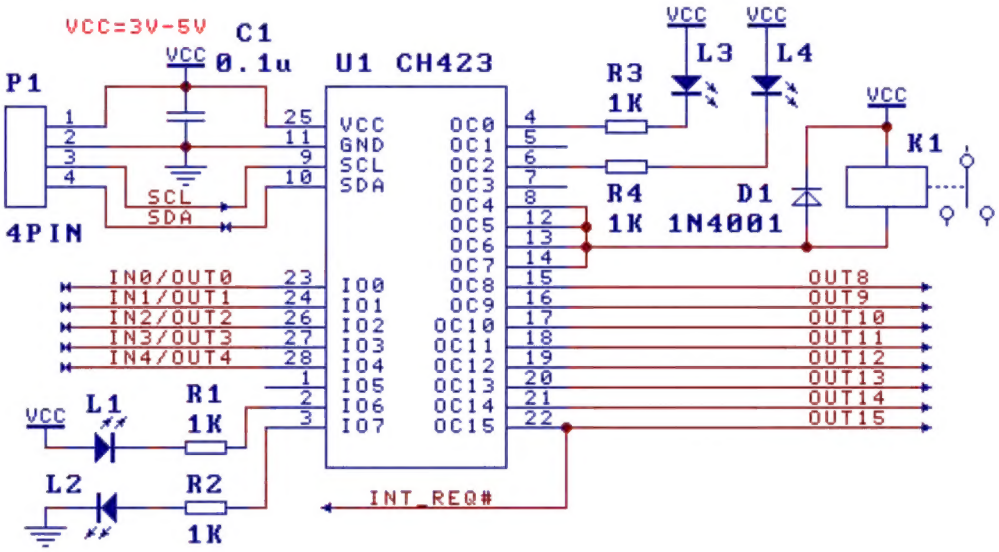


# 8. Application

## 8.1. Remote I/O Expansion (Figure below)

CH423 is connected to the external MCU through 2-wire serial interfaces SCL and SDA, and capacitor C1 is used for power supply decoupling.

The IO7~IO0 pins of CH423 can be used for input or output. In the figure, the IO6 and IO7 pins are used to drive LED light-emitting tubes of two polarities. The OC15~OC0 pins of CH423 can only be used for output. In order to obtain a larger continuous current driving capability, the open-drain output can be enabled, and the OC4, OC5, OC6, and OC7 pins are connected in parallel to drive relay K1 as shown in the figure.

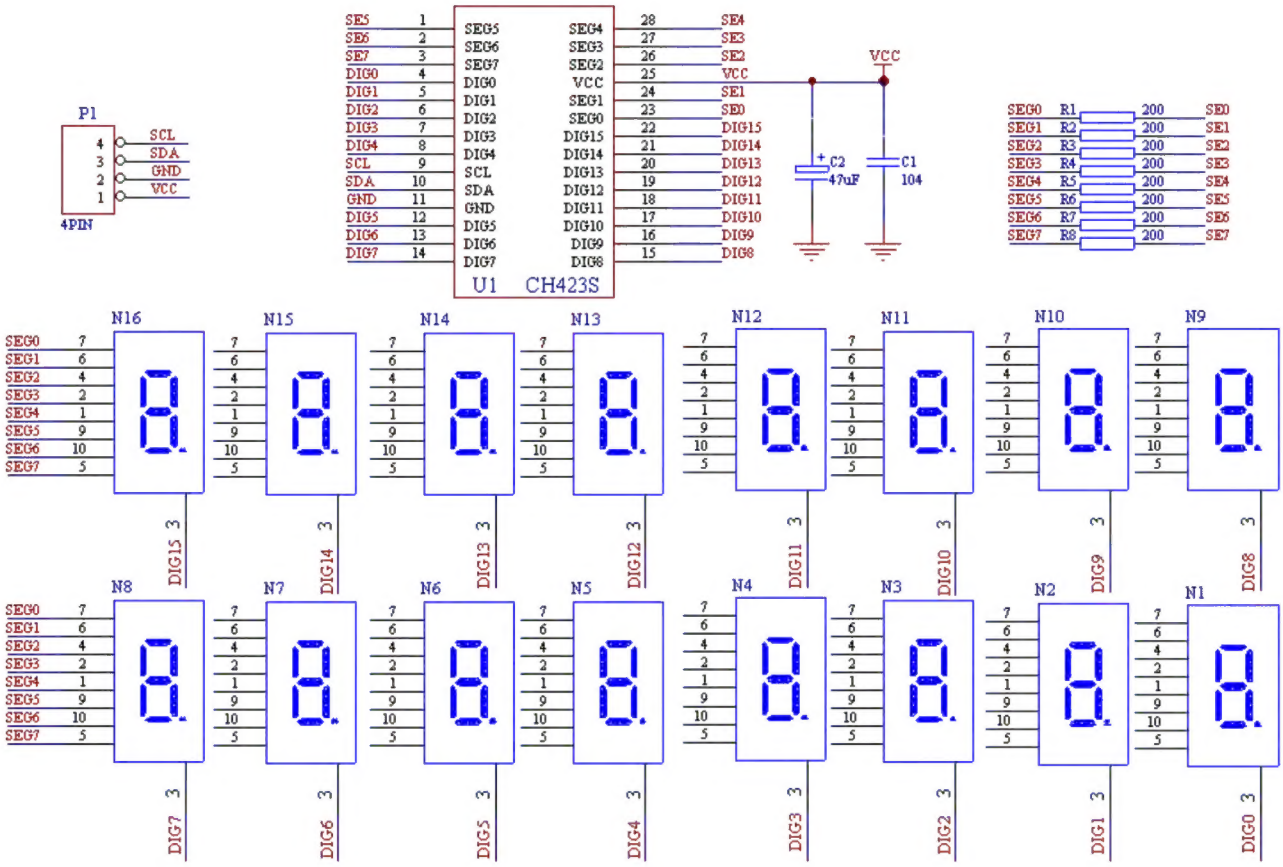



## 8.2. Dynamic Display Driver (Figure below)

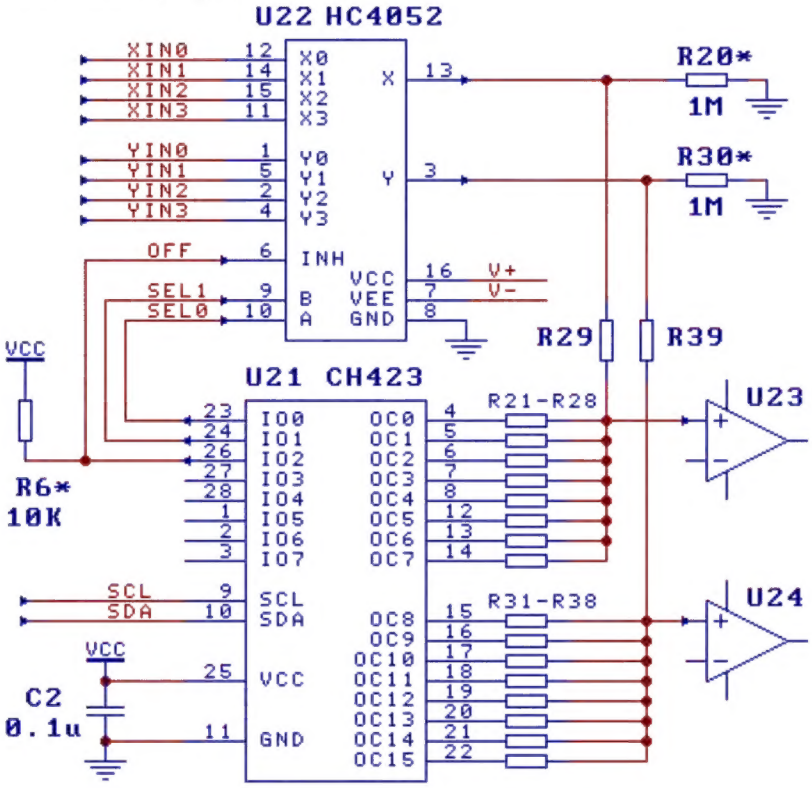
The dynamic display driving mode of CH423 is used to drive 128 LEDs or 16 common cathode digital tubes. The IO7 ~ IO0 pins drive each segment pin of the common cathode digital tubes (each digital tube is connected in parallel). The OC15 ~ OC0 pins drive the common terminal of each common cathode digital tube respectively. After MCU loads all word data, it turns on the DEC_L and DEC_H control bits and CH423 automatically performs time-sharing dynamic display scanning.

If you only need to drive 8 digital tubes, you can only turn on one control bit of DEC_L or DEC_H, and the remaining 8 general-purpose output pins can still be used for general-purpose output.

Since CH423 can limit the segment drive current internally, the current limiting resistors R1~R8 connected in series with the segment pins can be omitted.




## 8.3. Digital Potentiometer (Figure below)




The OC pin of CH423 is a low-resistance open-drain output in the open-drain output mode. The on-resistance is

less than 10Ω. It can be used as an analog switch with one end connected to the ground. Multiple OC pins can be connected to external resistors and combined to turn on. Digitally programmable resistor with one end connected to ground.

For example, a digital potentiometer can be formed by connecting 9 external resistors. After any combination of 8 resistors in parallel, a maximum of 256 resistance values can be obtained, from which no less than 32 effective resistance values can be selected (the resistance value increases in a certain way. requirements). The picture below is a dual-channel digital potentiometer composed of 18 external resistors. The MCU controls the resistors R21~R28 to conduct independently to the ground through CH423, and obtains a programmable pull-down resistor with a resistance of 256 levels. After the pull-down resistor divides the voltage with R29, generate a programmable voltage divider output and provide it to the subsequent operational amplifier U23, realizing the function of a digital potentiometer. R31~R39 in the figure constitute another channel.

U22 in the picture is a 4-to-1 analog switch. The MCU controls the analog switch to select the input channel through CH423, and then the nine resistors R21~R29 perform programmable voltage division and output. The optional pull-up resistor R6 in the picture is used to set the analog switch U22 to the off state by default during power-on reset. The optional resistors R20 and R30 in the picture are used to prevent the output signal from floating when the analog switches U22 and CH423 are both turned off.

The resistance value of each voltage divider resistor in the diagram should be determined according to the actual need, for example, R29 (R39) selects 4.7KΩ, and R21 to R28 (R31 to R38) selects 220Ω, 470Ω, 1KΩ, 2.2KΩ, 4.7KΩ, 10KΩ, 22KΩ, and 47KΩ, respectively, so that the minimum voltage divider output is 2.4% (when the OC pins are all on) and the maximum is 100% (when OC pins are all off), with an adjustment range of about 40 times.

## 8.4. Anti-interference (important)

Since the driving current of CH423 is large, it will produce a large glitch voltage on the power supply. Therefore, if the PCB layout of the power line or ground wire is unreasonable, it may affect the stability of MCU or CH423. Solutions to power supply interference:

①、It is recommended to use shorter and thicker power and ground wires, especially when the CH423 and MCU belong to two separate PCBs;

②、Connect a power supply decoupling capacitor in parallel between the positive and negative power supplies close to CH423, at least a 0.1uF capacitor and an electrolytic capacitor.

For external interference when the signal line is long, refer to the figure below to solve the problem:

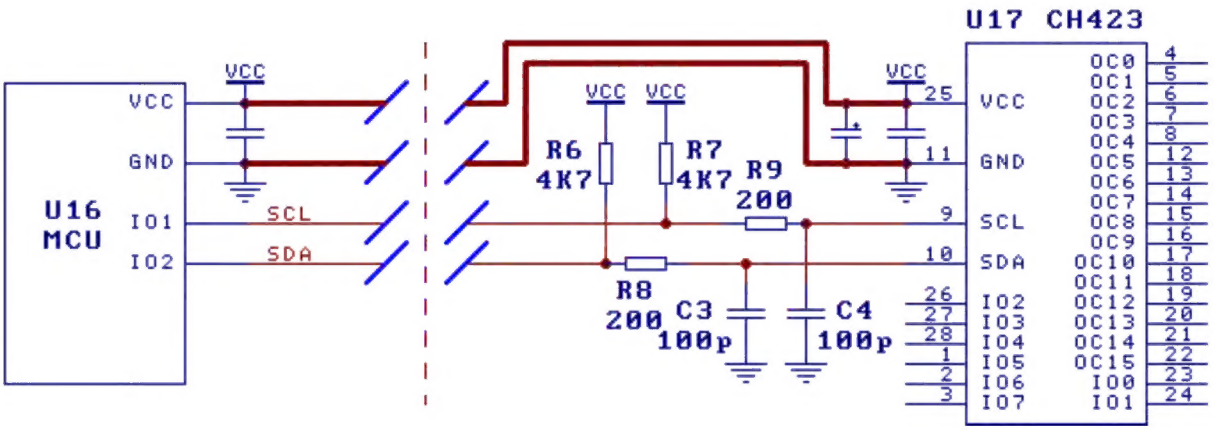
①、On the signal line close to the CH423 pin, add capacitors C3 and C4. The capacitance value can be 47pF to 470pF. The larger the capacitance, the slower the transmission speed of the communication interface with MCU;

②、Optionally add resistors R8 and R9, the resistance value can be 100Ω to 470Ω;

③、Reduce the transmission speed between MCU and CH423 (because of the increased resistance and capacitance);

④、If it is driven by a quasi-bidirectional I/O pin (such as a standard MCS51 MCU), it is recommended to add resistors R6 and R7. The resistance value can be 500Ω to 10KΩ to strengthen the pull-up of the quasi-bidirectional I/O pin of the MCS-51 MCU. Ability to maintain a better digital signal waveform during long-distance transmission; pull-up resistors R6 and R7 are not required when the signal line is short. For bidirectional I/O pins in totem pole driving mode, pull-up resistors R6 and R7 are not required.

In addition, for application environments with strong interference, the MCU can regularly refresh CH423 every few seconds, including reloading the output registers of each I/O pin and resetting system parameters.




## 8.5. MCU Interface Program

The website provides C language and ASM assembly interface programs for some MCU.